In the claims:

Claims 1-41 (canceled)

Claim 42 (currently amended) A semiconductor wafer which comprises:

a plurality of integrated circuits, each of said integrated circuits separated from the other of said integrated circuits by a scribe region at the periphery of each said integrated circuit; each of said integrated circuits including:

a centrally disposed core region;

at least one bond pad disposed between said core region and said scribe region;

an electrostatic discharge device; and

an I/O buffer disposed between said scribe region and said core region and laterally of said bond pad relative to said core region and said scribe region.

Claim 43 (previously presented) A semiconductor wafer which comprises:

a plurality of integrated circuits, each of said integrated circuits separated from the other of said integrated circuits by ascribe region at the periphery of each said integrated circuit; each of said integrated circuits including:

a centrally disposed core region;

at least one bond pad disposed between said core region and said scribe region;

an electrostatic discharge device disposed at least partially beneath said bond pad; and

an I/O buffer disposed between said scribe region and said core region.

Claim 44 (previously presented) The semiconductor wafer of claim 43 wherein said I/O buffer is further disposed laterally of said bond pad relative to said region and said scribe region.

Claim 45 (previously presented) An integrated circuit which comprises:

a semiconductor substrate which includes a scribe at the periphery of said substrate and a centrally disposed core region;

at least one bond pad disposed between said core region and said scribe region;

an electrostatic discharge device; and

an I/O buffer disposed between said scribe region and said core region and laterally of said bond pad relative to said core region and said scribe region.

Claim 46 (previously presented) An integrated circuit which comprises:

a semiconductor substrate which includes a scribe at the periphery of said substrate and a centrally disposed core region;

at least one bond pad disposed between said core region and said scribe region;

an electrostatic discharge device disposed at least partially beneath said bond pad; and

an I/O buffer disposed between said scribe region and said core region.

47. (previously presented) The circuit of claim 46 wherein said I/O buffer is further disposed laterally of said bond pad relative to said core region and said scribe region.

Claim 48 (previously presented) A method of fabricating a semiconductor wafer which comprises the steps of:

providing a plurality of integrated circuits, each of said integrated circuits separated from the other of said integrated circuits by a scribe region at the periphery of each said integrated circuit; and providing in each of said integrated circuits:

a centrally disposed core region;

at least one bond pad disposed between said core region and said scribe region;

an electrostatic discharge device; and

an I/O buffer disposed between said scribe region and said core region and laterally of said bond pad relative to said core region and said scribe region.

Claim 49 (previously presented) A method of fabricating a semiconductor wafer which comprises the steps of:

providing a plurality of integrated circuits, each of said integrated circuits separated from the other of said integrated circuits by a scribe region at the periphery of each said integrated circuit; and providing in each of said integrated circuits:

a centrally disposed core region;

at least one bond pad disposed between said core region and said scribe region;

an electrostatic discharge device disposed at least partially beneath said bond pad; and

an I/O buffer disposed between said scribe region and said core region.

Claim 50. (previously presented) The method of claim 49 wherein said I/O buffer is further disposed laterally of said bond pad relative to said core region and said scribe region.

Claim 51 (previously presented) A method of fabricating an integrated circuit which comprises the steps of:

providing a semiconductor substrate which includes a scribe at the periphery of said substrate and a centrally disposed core region;

providing at least one bond pad disposed between said core region and said scribe region;

providing a electrostatic discharge device; and

providing an I/O buffer disposed between said scribe region and said core region and laterally of said bond pad relative to said core region and said scribe region.

Claim 52 (previously presented) A method of fabricating an integrated circuit which comprises the steps of:

providing a semiconductor substrate which includes a scribe at the periphery of said substrate and a centrally disposed core region;

providing at least one bond pad disposed between said core region and said scribe region;

providing a electrostatic discharge device disposed at least partially beneath said bond pad; and

providing an I/O buffer disposed between said scribe region and said core region.

Claim 53 (previously presented) The method of claim 52 wherein said I/O buffer is further disposed laterally of said bond pad relative to said core region and said scribe region.